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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,409	01/14/2004	Hirotaka Kawata	118006	2629

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,409	KAWATA ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8-11,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-11,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 8-11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6433767 to Murade in view of US 6528358 to Murade et al.

Regarding claim 1, Murade discloses a transistor in fig. 3, comprising: a substrate 10, a capacitor line 3b, a semiconductor layer 1a including a channel region, column 15 line 31, a lightly doped region 1b, col. 15 line 31, a heavily doped region 1d, column 16 line 49, and a capacitor electrode region 1f, col. 16 line 21, the semiconductor layer 1a having a surface, a side extending substantially perpendicular

to the surface, and a gate insulating film 2 provided over the semiconductor layer 1a and under the capacitor line 3b, the gate insulating film having a total thickness set in a range of 20-150 nm, col. 25 line 33, and including a thermal oxide film,, col. 25 line 41, formed on the semiconductor layer 1a, the gate insulating film covering an area including at least the channel region, the lightly doped region 1b, and the heavily doped region 1d of the , fig. 3, a capacitor being formed by the capacitor line 3b, the capacitor electrode region 1f, and a dielectric including portions of the gate insulating film 2, a light-shielding layer 11a disposed between the substrate 10 and the semiconductor layer 1a at a position corresponding to the semiconductor layer 1a, the light-shielding layer 11a being formed from a conductive material selected from the group consisting of a simple metal substrate, an alloy, and a metal silicide including at least one of Ti, Cr, W, Ta, Mo, and Pb, col. 15 line 62; and an interlayer insulating film 12, col. 16 line 8, that electrically insulates the semiconductor layer 1a from the light shielding layer 11a.

But, Murade does not disclose a monocrystalline semiconductor layer having a shoulder portion disposed where the surface and the side intersect; a gate insulating film including a thermal oxide film formed on the monocrystalline semiconductor layer to a thickness in a range of 5nm to 50 nm, the thermal oxide film being thinner at a portion corresponding to the shoulder portion of the monocrystalline semiconductor layer than that at other portions, and at least one vapor-deposited insulating film, formed on the thermal oxide film, the at least one vapor-deposited insulating film covering an area including at least the channel region, the lightly doped region, and the heavily doped region of the

monocrystalline semiconductor layer, the at least one vapor-deposited insulating film having a thickness at the shoulder portion of the monocrystalline semiconductor layer that is substantially equal to that at other portions.

However, Yamazaki discloses a transistor in fig. 23A-E comprising: a substrate 39, col. 44 line 32, a monocrystalline semiconductor layer 41, column 44 line 32 and col. 47 lines 13-25, including a channel region 52, column 45 line 31, a lightly doped region 50, column 45 line 25, and a heavily doped region 49, column 45 line 16, the monocrystalline semiconductor layer 41 having a surface, a side extending substantially perpendicular to the surface, fig. 23A, and a shoulder (corner of layer 41) portion disposed where the surface and the side intersect, fig. 23A, and a gate insulating film 38/42 provided over the monocrystalline semiconductor layer 41, the gate insulating film having a thermal oxide film 38, column 44 line 33, formed on the monocrystalline semiconductor layer 41 to a thickness in a range of 5nm to 50 nm, col. 42 line 18, the thermal oxide film being thinner at a portion corresponding to the shoulder portion of the monocrystalline semiconductor layer 41 than that at other portions, and at least one vapor-deposited insulating film 42, column 44 line 38, formed on the thermal oxide film 38, fig. 23B, the at least one vapor-deposited insulating film 42 covering an area including at least the channel region 52, the lightly doped region 50, and the heavily doped region 47 of the monocrystalline semiconductor layer 41, fig. 23E, the at least one vapor-deposited insulating film having a thickness at the shoulder portion of the monocrystalline semiconductor layer 41 that is

substantially equal to that at other portions, fig. 23E. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use thermal oxide layer and vapor-deposited layers teaching of Yamazaki to replace the insulating film 2 of Murade, because it would have improved the device reliability and high mobility as taught by Yamazaki in col. 4 lines 25-30.

Regarding claim 2, Murade does not disclose the transistor wherein the monocrystalline semiconductor layer being made of monocrystalline silicon.

However, Yamazaki discloses the transistor according to claim 1, the monocrystalline semiconductor layer 38 being made of monocrystalline silicon, column 44 line 33 and discussion in claim 1 above for the same reason as discussed in claim 1

Regarding claim 3, Murade discloses the transistor the semiconductor layer 1a being a mesa type, fig. 3.

Regarding claim 4, Murade discloses the transistor wherein the semiconductor layer 1a having a thickness of 30-150 nm, column 25 line 31.

Regarding claims 8-11 and 15, Murade discloses an electro-optical device, comprising: a transistor 30 wherein a transistor being provided as a switching element, col. 12 line 57, in a display area, a electro-optical device, a semiconductor device, 15 or 19.

In the recitation 'an electro-optical device' and 'an electronic apparatus' has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the

portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478(CCPA 1951).

Regarding claim 16, Murade discloses the transistor further comprising a capacitor line 3b, the semiconductor layer 1a further having a storage capacitor electrode portion 1f that includes the shoulder portion, the thermal oxide film 2 interposed on the capacitor electrode portion 1f and serving as a dielectric, fig. 3.

But Murade does not disclose the vapor-deposited insulating being interposed between the capacitor line and the storage capacitor electrode portion.

However, as discussed in the above claim 1 Yamazaki discloses an insulating film comprising a thermal oxide layer the gate insulating film having a thermal oxide film 38, column 44 line 33, and a vapor-deposited insulating film 42, column 44 line 38, formed on the thermal oxide film 38, fig. 23B. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use thermal oxide layer and vapor-deposited layers teaching of Yamazaki to replace the insulating film 2 of Murade, because it would have improved the device reliability and high mobility as taught by Yamazaki in col. 4 lines 25-30.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

05 Dec. 2006

THAO X. LE
PRIMARY PATENT EXAMINER